WHAT IS CLAIMED is:

1. A semiconductor memory device comprising:

a plurality of bit line pairs each having first and second bit lines arranged in a first direction;

a cell array having a plurality of SRAM cells each of which is connected between the first and second bit lines of a corresponding bit line pair via first and second storage nodes, respectively;

a plurality of word lines arranged in a second direction crossing the first direction; and

a data write circuit which, in the write mode, writes data into an SRAM cell selected by a word line via the first and second bit lines and, in the read mode, rewrites data read onto the first bit line from an SRAM cell selected by a word line onto the first bit line.

2. The semiconductor memory device according to claim 1, wherein the write circuit includes a rewrite circuit which, when data corresponding to a precharge potential is read from the first bit line in the read mode, recharges the first bit line to the precharge potential on the basis of the read data.

3. The semiconductor memory device according to claim 1, wherein the write circuit includes a stop circuit which stops the operation of rewriting read data onto the bit line until read data is outputted to a data read output terminal in the read mode.

4. The semiconductor memory device according to claim 3, wherein the stop circuit includes a delay circuit which delays the operation of rewriting read data onto the bit line until read data is outputted to a data read output terminal in the read mode.

5. The semiconductor memory device according to claim 3, wherein the write circuit includes a precharge circuit which precharges the bit lines at times prior to the start of the read and write modes.

6. The semiconductor memory device according to claim 4, wherein the write circuit includes a precharge circuit which precharges the bit lines at times prior to the start of the read and write modes.

7. A semiconductor memory device comprising:

a plurality of bit line pairs each having first and second bit lines arranged in a first direction;

a cell array having a plurality of SRAM cells each of which is connected between the first and second bit lines of a corresponding bit line pair via first and second transfer gates having first and second storage nodes, respectively;

first and second word lines arranged in a second direction crossing the first direction and connected to the first and second transfer gates, respectively; and

a data write circuit which, in the write mode, writes data into an SRAM cell selected by the first and second word lines via the first and second bit lines

and, in the read mode, rewrites data read onto at least one of the first and second bit lines from an SRAM cell selected by an activated one of the first and second word lines onto the bit line onto which the data has been read.

8. The semiconductor memory device according to claim 7, wherein the write circuit includes a rewrite circuit which recharges one of the first and second bit lines to a precharge potential onto which data corresponding to a precharge potential has been read in the read mode.

9. The semiconductor memory device according to claim 7, wherein the write circuit includes a stop circuit which stops the operation of rewriting read data onto the bit line until read data is outputted to a data read output terminal in the read mode.

10. The semiconductor memory device according to claim 9, wherein the stop circuit includes a delay circuit which delays the operation of rewriting read data onto the bit line until read data is outputted in the read mode.

11. The semiconductor memory device according to claim 9, wherein the write circuit includes a precharge circuit which precharges the bit lines at times prior to the read and write modes.

12. The semiconductor memory device according to claim 10, wherein the write circuit includes

a precharge circuit which precharges the bit lines at times prior to the read and write modes.